In The Specification

Please replace the paragraph beginning on page 2, line 13, with the following rewritten paragraph:

In anisotropically etching contact or via holes (openings), plasmas containing fluorocarbons or hydrofluorocarbons including oxygen and nitrogen are typically optimized in various steps in a plasma etching process to selectively etch through the various layers of materials included in a multi-layer semiconductor device. For example, it is typically required to selectively etch through an oxide containing layer, for example an IMD layer to a desired depth. Frequently, etching stop layers, for example, ~~metal~~ nitride or silicon carbide, are formed in the substrate for several reasons including providing a material non-selective to an etching chemistry to protect an underlying layer and to provide a dissimilar material for plasma etching endpoint detection to reliably etch to a particular depth. In addition, an etching stop layer functions as a hard mask resistant to an etching chemistry to reduce undesired isotropic etching in overlying layers.

Please replace the paragraph beginning on page 4, line 4, with the following rewritten paragraph:

Referring to Figure 1A, for example, is a typical dual damascene structure following via opening etching and trench etching. In a typical dual damascene processing approach it has been useful to form an etching stop layer between the trench layer and the via layer forming the trench /via interface. Following this approach, a substrate is provided, for example, having a conductive area 12A formed in an insulating layer 12B. Overlying the conductive area 12A and insulating layer 12B is formed a first etching stop layer 14A and a via insulating layer 16A for etching a via therein. Overlying the via insulating layer 16A is a second etching stop layer 14B. One approach in forming the dual damascene structure is to form a trench insulating layer 16B, followed by a third etching stop layer 14C which is photolithographically patterned and etched to form a via opening e.g., 20A that extends through the substrate to the conductive area 12A. Following formation of the via opening 20A, the photolithographic patterning process is repeated to etch a trench opening e.g., 20B formed substantially over the via opening e.g., 20A. The first, second, and third etching stop layers 14A, 14B, and 14C are typically formed of a ~~metal~~ nitride or ~~metal~~ carbide including for example, silicon nitride(e.g., Si_3N_4), silicon carbide (e.g., SiC), and silicon oxynitride

(e.g., SiON). In a typical plasma etching process the etching stop layers e.g., 14A, 14B, and 14C are advantageously used to detect an etching depth, for example, by optical detection of etched plasma species and provide an increased etching selectivity, e.g., 14B and 14C, while etching the insulating layer to maintain a uniform etching profile. For example, when etching the trench opening e.g., 20B, the etching stop layer 14B protects the via opening 20A from isotropic etching when the trench etching depth reaches the etching stop layer 14B.

Please replace the paragraph beginning on page 5, line 16, with the following rewritten paragraph:

One shortcoming of the above approach is the presence of relatively high dielectric constant (e.g., > 6.5) ~~metal~~ nitride or ~~metal~~ carbide etching stop layers which undesirably add to the overall capacitance of the multi-layer structure thereby increasing parasitic electrical contributions to signal delay times. Another drawback of forming etching stop layers between the insulating layers (IMD/ILD layers), which are frequently porous to reduce the dielectric constant of the insulating layer, is that poor adhesion between the etching stop and IMD layer results leading to reduced multi-layer strength and in many cases, peeling during subsequent chemical mechanical polishing processes. In an effort to overcome these shortcomings and

drawbacks, another approach to dual damascene processing has been to eliminate etching stop layers including at the trench/via interface e.g., 14B, in the processing scheme. In this approach, referring to Figure 1B, only one insulating layer is provided e.g., 16C for etching both the via opening 20A and trench opening 20B. In this approach, the trench etching process typically proceeds for a predetermined period of time in contrast with end-point detection provided by an etching stop layer, e.g., 14B in Figure 1A. With the many etching variable involved in plasma processing, it has proven difficult to achieve consistent trench etching results by using a predetermined process window (etching time) for trench etching.

Please replace the paragraph beginning on page 10, line 6, with the following rewritten paragraph:

While the method of the present invention is explained in with reference to plasma etching of trench line openings in a dual damascene process it will be appreciated that the present invention may be applied to the etching of any semiconductor feature where the requirement of an etching stop layer may be avoided by including an etching stop liner according to the present invention to improve an etching stop profile and/or for providing an alternative endpoint detection means. For example, ~~providing~~ an etch stop liner may be provided in etched contact

holes or vias in a stacked borderless process for creating vias and metal interconnects in a semiconductor manufacturing process.

Please replace the paragraph beginning on page 11, line 5, with the following rewritten paragraph:

For example, referring to Figure 2A, is shown a cross sectional side view of portion of a multilayer semiconductor device included in a semiconductor wafer showing a substrate 22 for creating for example, a via in a dual damascene structure at a stage in the manufacturing process. The substrate 22 includes a first insulating layer 22A with, for example, a conductive area 22B formed therein. Overlying the first insulating layer 22A and conductive area 22B, is typically formed a first etching stop layer 24A including a ~~metal~~ nitride or ~~metal~~ carbide material, for example, silicon nitride (e.g., Si_3N_4), silicon carbide (e.g., SiC), or silicon oxynitride (e.g., SiON). The etching stop layer 24A is typically deposited by a (chemical vapor deposition (CVD) process including for example, PECVD (plasma enhanced CVD), LPCVD (low pressure CVD), or HDPCVD (high density plasma CVD) under conditions that are well known in the art. A typical thickness of the etching stop layer 24A, for example, is between about 300 and 1000 Angstroms.

Please replace the paragraph beginning on page 12, line 4, with the following rewritten paragraph:

Overlying the first etching stop layer 24A is an inter-metal dielectric (IMD) layer 26 (insulating layer) for subsequently etching a semiconductor feature, for example, a via opening, the IMD layer being formed of, for example, silicon dioxide, or a low-k doped silicon dioxide. Typically, the dielectric constant of the low-k material is less than about 3.0 to minimize electrical parasitic capacitive effects. It will be appreciated that other low-k materials may be used and that the method according to the present invention is likewise applicable to those materials, particularly if they are porous materials. Additional exemplary low-k inorganic materials include, for example, doped and undoped porous oxides, xerogels, or SOG (spin-on glass). Exemplary low-k organic materials include, for example, polysilsesquioxane, parylene, polyimide, benzocyclobutene, amorphous Teflon, and spin-on polymer (SOP).

Please replace the paragraph beginning on page 13, line 1, with the following rewritten paragraph:

Overlying the IMD layer 26 is a second etching stop layer 24B, formed of, for example, a ~~metal~~ nitride or ~~metal~~ carbide including silicon nitride, silicon carbide, or silicon oxynitride. The etching stop layer 24B functions as a hard mask for controlling the etching profile of a subsequently etched via opening. Optionally formed over the second etching stop layer 24B, is a dielectric anti-reflective coating (DARC) layer (not shown) to reduce light reflectance in a subsequent photolithographic patterning step of subsequently deposited photoresist layer 28A. The optional DARC layer is typically a silicon oxynitride layer which can be optically optimized by varying oxygen content.

Please replace the paragraph beginning on page 15, line 11, with the following rewritten paragraph:

According to the present invention, the etching stop liner 32 is preferably formed of a ~~metal~~ nitride or ~~metal~~ carbide including for example, ~~silicon for example,~~ silicon nitride (e.g., Si_3N_4), titanium nitride (e.g., TiN), silicon carbide (e.g., SiC), or silicon oxynitride (e.g., SiON). The etching stop liner is preferably deposited by a chemical vapor deposition

(CVD) process or a spin on process by methods known in the art. For example, in a CVD process the deposition process may include, for example, PECVD (plasma enhanced CVD), LPCVD (low pressure CVD), or HDPCVD (high density plasma CVD) by reacting a ~~metal-metal-organic~~ precursor with a nitrogen containing or carbon containing precursor by methods that are known in the art. The etching stop liner 32 is preferably deposited to a thickness of about 50 Angstroms to about 500 Angstroms.

Please replace the paragraph beginning on page 19, line 16, with the following rewritten paragraph:

Referring to Figure 4 is shown a general process flow diagram encompassing several embodiments of the present invention. Beginning with process 401, a via patterning and etching process is carried out on a substrate, in one embodiment an IMD layer without an etching stop liner interposed between a trench line portion and a via portion (i.e., via formed in a continuous portion of the insulating (IMD) layer). Following process 401, an etching stop liner is formed according to process 403 by blanket depositing an etching resistant material, preferably a ~~metal~~ nitride or ~~metal~~ carbide, to at least partially cover the via opening sidewalls. Following process 403 in a preferred but optional embodiment, a via plug is formed according to process 405 to at least partially fill the via

opening, preferably to a level at least about equal to a subsequently etched trench line depth. Following either process 405 or 403, a trench line patterning and etching process according to process 407 is performed to complete the formation of the dual damascene etching process.